

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Attorney Docket No.: CYPR-CD03007

Inventor(s): Sancheti et al.

Group Art Unit:

Filed: 03/18/04

Examiner:

Application No.: 10/804,988

Title: A DELAY CIRCUIT THAT SCALES WITH CLOCK CYCLE TIME

Commissioner of Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

Information Disclosure Statement Submitted Pursuant to 37 C.F.R. 1.97(b)

The citations referenced herein, copies attached, may be material to the examination of the above-identified application and are, therefore, submitted in compliance with the duty of disclosure as defined in 37 C.F.R. 1.56. The Examiner is requested to make these citations of official record in the application.

This Information Disclosure Statement submitted in accordance with 37 C.F.R. 1.97(b) is not to be construed as a representation that a search has been made, that additional items material to the examination of this application do not exist, or that any one or more of these citations constitute prior art under 35 U.S.C. 102.

The Examiner's attention is respectfully directed to the following U.S. Patents:

<u>Pat. No.</u>	<u>Pat. Title</u>	<u>Grant Date</u>
6,819,157	DELAY COMPENSATION CIRCUIT	11/16/04
6,445,661	CIRCUIT, DISK CONTROLLER AND METHOD FOR CALIBRATING A HIGH PRECISION DELAY OF AN INPUT SIGNAL	09/03/02
6,445,238	METHOD AND APPARATUS FOR ADJUSTING DELAY IN A DELAY LOCKED LOOP FOR TEMPERATURE VARIATIONS	09/03/02
6,327,318	PROCESS, VOLTAGE, TEMPERATURE INDEPENDENT SWITCHED DELAY COMPENSATION SCHEME	12/04/01
6,175,928	REDUCING TIMING VARIANCE OF SIGNALS FROM AN ELECTRONIC DEVICE	01/16/01
6,100,739	SELF-TIMED SYNCHRONOUS PULSE GENERATOR WITH TEST MODE	08/08/00
6,043,717	SIGNAL SYNCHRONIZATION AND FREQUENCY SYNTHESIS SYSTEM CONFIGURABLE AS PLL OR DLL	03/28/00

Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation	
							Yes	No
	H	JP404227314	08/17/92	JP	H03K005	13		x

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Date: 7 Sept. 2005

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Form 1449

U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
	A	6,819,157	11/16/04	Cao et al.	327	262	11/15/01
	B	6,445,661	09/03/02	Wu	369	59.2	08/11/99
	C	6,445,238	09/03/02	Lesea	327	262	12/01/99
	D	6,327,318	12/04/01	Bhullar et al.	375	374	06/30/98
	E	6,175,928	01/16/01	Liu et al.	713	401	12/31/97
	F	6,100,739	08/08/00	Ansel et al.	327	175	09/09/98
	G	6,043,717	03/28/00	Kurd	331	17	09/22/98

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							Yes	No
	H	JP404227314	08/17/92	JP	H03K005	13		X

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
	I	
Examiner		Date Considered

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered.
Include copy of this form with next communication to applicant.